1. Refreshing a DRAM array is accomplished by sequentially doing a dummy read on each row in the DRAM. Assume a 256 Mb DRAM bank that is organized as a square with the same number of column and row addresses. (Recall that all cells in a row are refreshed at the same time.) Assume that each cell needs to be refreshed every 90 msec and that the read cycle time is 100 nsec. Calculate the percentage of time that the DRAM bank is busy refreshing.

2. Assume that all memory systems use byte addressable memory and cache virtual memory addresses of size 32b. Give the split up of the memory address in tag, index, et ceter., indicate the layout of a cache line, and calculate the storage overhead for the following L3 caches.
   a. Direct Mapped Cache with Copy Back of size 256MB.
   b. Block Cache with block size 16B, Copy Back, size 256 MB.