1. Explain at least two different ways in which the speed of a storage device is evaluated.

2. Give the formula for the access time of a cache based on the cache miss rate, the miss penalty, and the cache access time. Explain all the terms in the equation.

3. Explain the idea behind set-associativity. How is set associativity implemented and what is the reason to implement it.

4. Draw a 4T2R SRAM cell and explain its functioning. Then draw a 6T SRAM cell and explain its functioning.

5. Explain the sequence of events that are involved in a read from a DRAM array.

6. A DRAM bank contains 256M cells. The array contains the same number of word and bit lines. A DRAM cell needs to be refreshed every 40 milliseconds. Assume that the refresh operation (basically a dummy read) takes 60 nanoseconds. Calculate the percentage of time that the DRAM bank is refreshing.

7. A L2 cache located between the processor and the main memory system can store 128MB data. It is four way set associative and stores blocks of four words. The cache uses random replacement instead of LRU and uses copy-back. Give the layout of an individual cache line (metadata and data), show how a virtual memory address of 32 bits is split, and calculate the overhead of metadata over data.

Use the provided white paper to give your answers. Initialize all answers.