The School of Engineering Honor's Code applies.

1. Give at least five criteria by which memory and storage is evaluated.

2. Explain the write-through and copy-back policies for cache writes. Explain their relative advantages and disadvantages using the L2 cache between processor and main memory as well as a DRAM cache on a hard drive as examples.

3. Draw a 1T1C DRAM cell. Draw a sketch that shows the main components of a DRAM design: row address decoder, column address decoder, word lines, bit lines, sense amplifiers, I/O port (or buffer), DRAM cells.

4. Explain the sequence of events that are involved in a read from a DRAM array, including the refresh.

5. A DRAM bank contains 64Mb cells. The array contains the same number of word and bit lines. A DRAM cell needs to be refreshed every 50 milliseconds. Assume that the refresh operation (basically a dummy read) takes 50 nanoseconds. Calculate the percentage of time that the DRAM bank is refreshing.

6. A L2 cache located between the processor and the main memory system can store 64MB data. It is two way set associative and stores blocks of four words. The cache uses random replacement instead of LRU and uses write-through. Give the layout of an individual cache line (metadata and data), show how a virtual memory address of 32 bits is split, and calculate the overhead of metadata over data.

Use the provided white paper to give your answers. Initialize all answers.