Problem 1:  [5pt]
Speed, Cost, Capacity, Reliability (Availability), Volatility. [1pt per item]

Problem 2:  [12pt]
Write-Through: A write is performed to both the cache and the underlying memory / storage element. [2pt.]
Copy-Back: A write is performed only to cache. A dirty bit or other marker is set to flag written data that differs from the copy in the underlying memory / storage element. If that item is moved from the cache, then it needs to be copied first to the underlying memory / storage unit. [2pt]

Advantages: Write-Through:
- There is no consistency problem between cache and main storage element. This is important for disks, but not important for main memory modules, which fail simultaneously with the cache. [2pt]
- There is no need for a dirty bit. This is visible in L2 cache overhead, but not that important for disks. [2pt]

Disadvantages: Write-Through:
- All writes stress the connection between cache and underlying unit. This is bad for disks that see an increase in the number of disk accesses to be performed, but not as bad for the connection between main memory and L2 cache. [2pt]
- Copy-back potentially increases the miss penalty, because one more operation has to be performed. This is not important for disks, but possibly for the L2 cache. [2pt]

Problem 3: [10pt]
(a) 5 pt.
(b) 5 pt.
   (a) No details in memory array –1
   (b) addr

Problem 4: [12pt]
- Precharge of bit lines.
- Row address decoded, word line asserted.
- Charge exchange between capacitor and bit line.
- Sense amplifiers are activated, pull up the voltage differential between read bit line and reference bit line.
- Column address is decoded and used to select one bit output.
- Word line is deasserted (recharging all the charges).

Problem 5: [12pt]
DRAM bank has \(2^{26}\) cells, hence \(2^{13}\) rows with \(2^{13}\) cells each. [4pt]
Every 50 millisecond, \(2^{13}\) rows need to be read, which takes \(2^{13} \times 50\) nsec. [4pt]
Proportion of refreshes is \[ \frac{2^{13} \cdot 50 \cdot 10^{-9}}{50 \cdot 10^{-3}} = 8.192 \cdot 10^{-3} = 0.8192\% . \] [4pt]

**Problem 6:** [12pt]
Each cache line contains 8 words or \(2^5\)B. The cache contains \(2^{26}B/2^5B = 2^{21} = 2M\) cache lines. [4pt]
The 32 address is split in 2b-byte-in-word + 2b-word-in-block + 21b-index + 7b-tag. [4pt]
A cache line consists of two 7b tags and 8*32b = 256b. The overhead is 14/256 or 2.7%. [4pt]